Development of an interleaved delta-sigma A/D converter optimized for multi-sensors

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custom IC, delta-sigma A/D converter, multi-sensors, digital filter

In industrial measurement equipment, accuracy is often enhanced using multi-sensor systems. For instance, pressure and temperature sensors are installed to perform corrections on the primary sensor and adjust data for environmental changes. When performing correction calculations, it is essential to reduce latency between multiple sensors and ensure A/D conversion with high precision and low power consumption. To address this challenge, we proposed an interleaved delta-sigma A/D converter optimized for multiple sensors, and conducted functional verification through the prototyping and evaluation of the circuit.

1. Introduction

In the field of industrial measuring instruments, multi-sensor systems using multiple sensors for correction are widely used to obtain high-precision measurement results. In pressure measurement, for example, secondary pressure sensors and temperature sensors are also employed to correct the characteristics of the primary pressure sensor.

Delta-sigma A/D conversion techniques [1],[2],[3] are commonly used for high-precision measurement. However, when commercially available delta-sigma A/D converters, which have large latency (time from input sampling to output A/D conversion results) between input channels, are used for A/D conversion of multiple sensors, correlation between the sensors cannot be established. This produces a large error when those results are used for correction. On the other hand, if multiple A/D converters are used simultaneously to reduce latency, the power consumption becomes excessive. For example, a measuring instrument operating with a current of 4 to 20 mA, such as two-wire field devices, is required to operate with a current consumption of 4 mA or less. Therefore, reducing the power consumption of A/D conversion functions is essential for implementing multiple functions in a product.

As mentioned above, in multi-sensor sensing, specifically in A/D converters, key challenges include maintaining correlation between multiple sensors and reducing latency and power consumption. To solve those issues, we designed a new A/D converter optimized for multi-sensor systems, implemented it as our proprietary custom IC, and evaluated its functionality. The results are reported below.

2. Application of delta-sigma ADC to multi-sensor systems

2.1 Basic architecture of delta-sigma ADC [1],[2],[3]

Delta-sigma A/D converters ("delta-sigma ADCs" from here on) are commonly used in analog interface circuits as high-precision A/D conversion circuits. As figure 1 shows, a delta-sigma ADC is composed of an integrator made up of analog circuits, a quantizer (comparator), a delta-sigma modulator that feeds back the difference with the input signal, and a digital filter in the downstream stage. The upstream delta-sigma modulator converts the input analog voltage into a digital modulation signal, and the downstream digital filter performs time-averaging and decimation (downsampling) of the digital modulation signal.

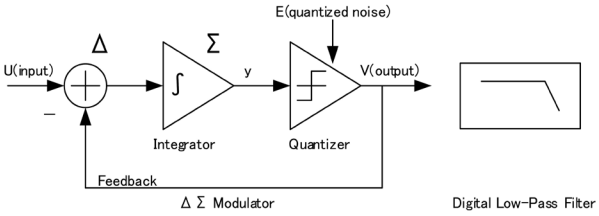

Fig. 1. Schematic diagram of a delta-sigma ADC

A delta-sigma ADC uses oversampling and noise shaping techniques to achieve high-precision A/D conversion. The principle is shown in figure 2.

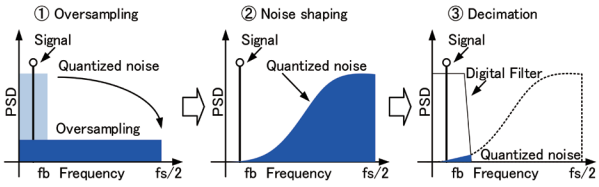

Fig. 2. Principle of achieving high SNR in delta-sigma ADC

Oversampling is a method of sampling an input signal at a rate

higher than the signal frequency range. Noise components such as thermal noise and quantization noise are distributed in the range up to the Nyquist frequency (half of the sampling frequency). Therefore, high-rate sampling can distribute the noise component over a wider frequency range, thereby reducing noise in the signal frequency range.

Noise shaping is a technique for distributing quantization noise generated in a quantization circuit to the higher frequency range. By forming a feedback loop to integrate the difference between the input signal and output modulation signal using a delta-sigma modulator, noise components in the low-frequency range are suppressed. Quantization noise shifted to the higher frequency range by noise shaping can be removed by averaging with a low-pass digital filter.

The effect of noise shaping increases with the number of times (order) the signal is integrated in the delta-sigma modulator, and quantization noise acquires a high-order high-pass characteristic. To remove quantization noise, the downstream digital filter needs to have a higher-order low-pass characteristic than the quantization noise. For example, when the order of the delta-sigma modulator is 2, the digital filter requires a third-order low-pass characteristic.

2.2 Digital filter latency

A circuit called a SINC filter is widely used as a digital filter for a delta-sigma ADC. As an example of a SINC filter, a SINC3 filter used for a second-order delta-sigma ADC is shown in figure 3.

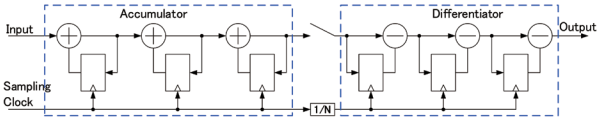

Fig. 3. Schematic diagram of SINC3 filter

A SINC3 filter is composed of three accumulators, a down-sampler (the switch in figure 3) and three differentiators, and has the advantage of being able to configure a high-order filter circuit with fewer circuit components than connecting multiple low-pass filters in a cascade. [4]

Let N be the ratio of the sampling frequency to the input signal frequency (i.e. oversampling ratio). A SINC3 filter outputs an A/D conversion result every N sampling cycles. However, delta-sigma modulator data for 3N sampling periods are required for averaging in the digital filter before an output is obtained again after the register circuit in the filter is reset, such as at the start of A/D conversion during power-up or when the input signal is switched. In other words, a data uptake period three times longer is required to obtain data immediately after reset. Figure 4 shows the latency required immediately after reset.

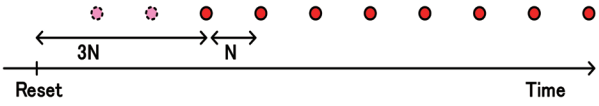

Fig. 4. Data update timing immediately after digital filter reset in a delta-sigma ADC

2.3 Application of delta-sigma ADC to multi-sensor systems

Figure 5 shows an application of delta-sigma ADCs to a multi-sensor system. When using a commercially available delta-sigma ADC, possible options include switching sensor inputs using a multiplexer, as shown on the left side of figure 5, or installing multiple delta-sigma ADCs according to the number of sensors, as shown on the right side of figure 5.

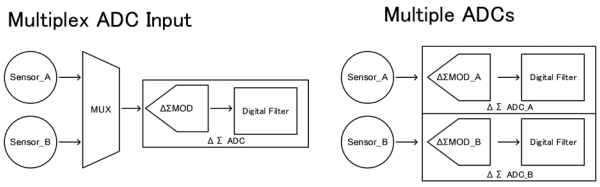

Fig. 5. Schematic diagram of application of delta-sigma ADCs to a multi-sensor system

Switching the sensor input requires resetting the digital filter at the switching timing. This means, as shown in Section 2.2, that a latency equal to three times the data update period occurs every time the input is switched. For example, when two sensor signals are A/D converted sample-by-sample as shown in figure 6, a latency equal to 3N sampling periods occurs in the delta-sigma modulator for every data output. As a result, the data update period for each sensor is equal to 6N sampling periods for the modulation signal, which is six times longer than a non-switching configuration.

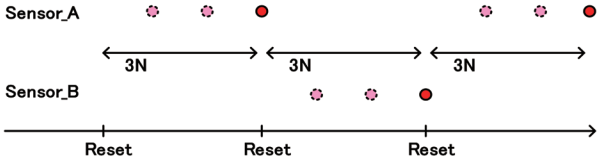

Fig. 6. Data update timing of multiple sensor A/D conversion

If multiple delta-sigma ADCs are incorporated according to the number of sensors, the latency shown in figure 6 does not occur because no switching is required. However, this technique requires multiple delta-sigma ADCs, which leads to increased power consumption. Therefore, product implementation is difficult when power consumption is restricted.

3. Interleaved delta-sigma ADC [6]

3.1 Circuit overview

To solve the problem shown in Section 2.3, we propose a circuit architecture that enables multi-channel A/D conversion without requiring resetting the digital filter and with a circuit scale equivalent to that of a delta-sigma modulator.

First, figure 7 shows the circuit diagram of a conventional delta-sigma modulator.

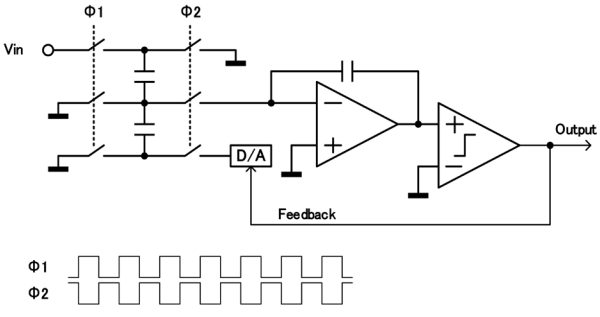

Fig. 7. Circuit diagram (top) and timing diagram (bottom) of a conventional delta-sigma modulator

The circuit shown in figure 7 is a circuit configuration called a switched capacitor. It receives an analog voltage as charges to its capacitors and integrates the input signal by toggling the switches between the open and closed states according to the timing shown in the timing diagram to charge and discharge the capacitors. In the conventional circuit, the integral of the input signal is stored as a charge in the integration capacitor connected to the inverting input terminal and output terminal of the operational amplifier.

The circuit diagram of the proposed delta-sigma modulator is shown in figure 8.

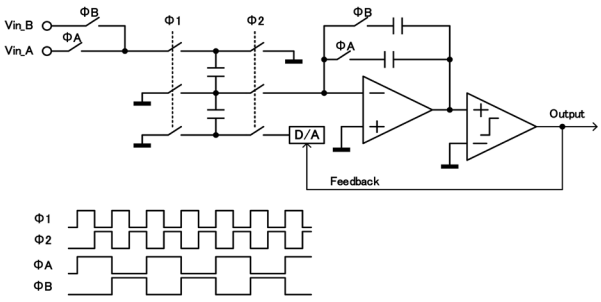

Fig. 8. Circuit diagram (top) and timing diagram (bottom) of a newly designed interleaved delta-sigma modulator

We call the newly designed circuit an interleaved delta-sigma modulator. Its features include a selection circuit that switches signals from multiple input channels, along with the use of integration capacitors equal in number to the input channels. For example, when integrating the input signal in channel A, the switch for channel A is closed and that for channel B is opened. During this time, the charge, i.e. the integral of the signal, of channel B is stored. By switching the selection of input channels A and B for each integration operation, as shown in the timing diagram in figure 8, it is possible to integrate multiple input channels in parallel.

We call an A/D converter with the proposed interleaved delta-sigma modulator an interleaved delta-sigma ADC. Figure 9 shows the configuration of a two-input circuit example.

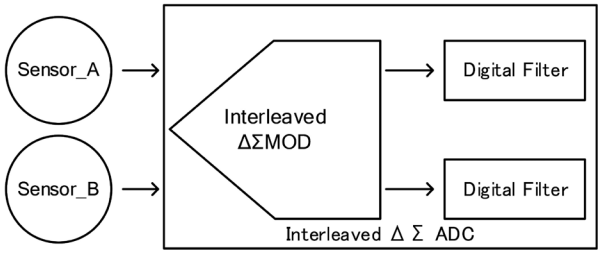

Fig. 9. Overall configuration of interleaved delta-sigma ADC

Because the interleaved delta-sigma modulator outputs modulation signals corresponding to the two input channels in parallel, two digital filters are required to be implemented in the downstream stage. Although in figure 9, two digital filters are shown in parallel for simplicity, the implementation is not a straightforward parallel configuration due to internal sharing. [4]

By using two digital filters to remove quantization noise and perform decimation (downsampling), multiple channels can be A/D converted without resetting. The data update timing of this interleaved delta-sigma ADC is shown in figure 10.

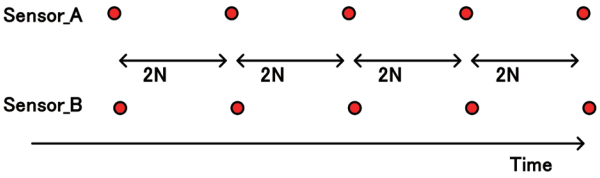

Fig. 10. Data update timing of interleaved delta-sigma ADC

Although it takes 2N sampling periods to output N points of modulation signal for each channel due to the alternate integration of two input channels, the latency shown in figure 6 does not occur in principle. This is because there is no need to reset the digital filters. The time difference between channels, which is approximately equal to the sampling period of the delta-sigma modulator used for oversampling, is sufficiently short for the time variation of the input signal.

3.2 Prototype circuit design

To verify the interleaved delta-sigma modulator shown in Section 3.1, we designed a prototype IC circuit and verified its operation through evaluation. Figure 11 shows the circuit diagram of the prototype interleaved delta-sigma modulator.

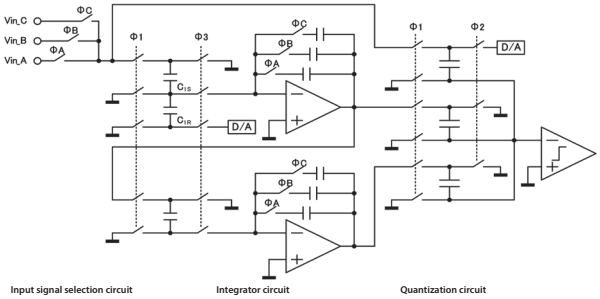

Fig. 11. Circuit diagram of the prototype interleaved delta-sigma modulator (partially simplified description)

The circuit in figure 11 was designed as a second-order delta-sigma modulator, [5] which integrates the difference between the input signal and the output modulation signal in two stages. The downstream quantization circuit A/D converts the signal obtained by adding the input signal and the outputs of the first- and second-stage integrator circuits, and the conversion result is fed back to the D/A converters of the integrator circuits.

In figure 11, for the sake of simplicity the circuit is described as having a single-ended input. However, the actual prototype circuit was designed as a differential input type to suppress common-mode noise in the input signal.

The sampling frequency of the delta-sigma modulator is 100 kHz. The power supply voltage is 3.3 V, and the current consumption is approximately 230 uA. The prototype circuit, which was designed to perform three-channel A/D conversion in parallel, is equipped with three channels of input signal selection circuits and integration capacitors. In this prototyping, of the three input channels A, B, and C, channel A was assigned to the main sensor requiring high precision, and channels B and C to sub sensors. To increase the average number of times channel A is processed, the channel switching sequence in parallel conversion was set to channel A → B → A → C. As a result, the sampling frequency of channel A is twice that of channels B and C, and the noise reduction effect of oversampling shown

in Section 2.1 increases. To control the timing so that the sampling and integration of an input signal take 10 us (100 kHz), the sampling period was set to 20 µs (50 kHz) for channel A, and 40 µs (25 kHz) for channels B and C.

3.3 Prototype circuit implementation and evaluation

To demonstrate the functionality of interleaved delta-sigma ADC, we prototyped an IC equipped with the circuit shown in figure 11 and evaluated its A/D conversion functionality. The prototype circuit inside the IC is shown in figure 12. The prototype circuit was designed using a 180-nm CMOS process.

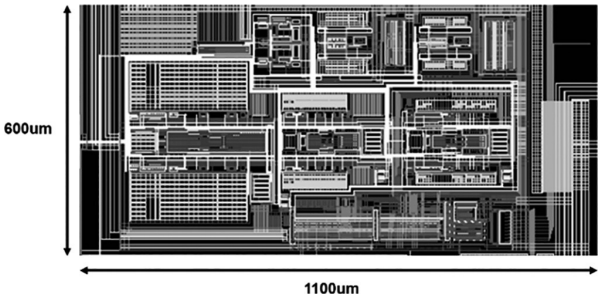

Fig. 12. Mask pattern of the prototype IC
(surrounding area of interleaved delta-sigma ADC)

Next, the evaluation of this prototype circuit is shown below.

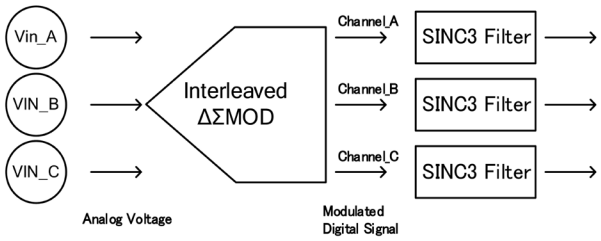

Fig. 13. Evaluation of interleaved delta-sigma ADC

DC voltages were applied to each of the three input terminals of the interleaved delta-sigma ADC, and after noise removal and downsampling were performed on the output modulation signal using SINC3 filters, A/D conversion results were obtained. Figure 13 shows a schematic diagram of this.

In the evaluation, we verified the multi-channel parallel A/D conversion function by checking whether the input voltages applied to each channel corresponded to the A/D conversion results. First, the mean and standard deviation of the A/D conversion results were calculated. Then, the gain (sensitivity) was derived from the relationship between the mean and input voltage, and the standard deviation was interpreted as the noise of the A/D converter.

To enable a fair comparison within the same input signal frequency range, the averaging length N of the SINC3 filter was set to 500 for channel A, and 250 for channels B and C so that the data update period was 10 ms.

Figure 14 shows the A/D conversion results for each channel, and figure 15 gives an enlarged view of the deviation of the A/D conversion results for channel A. The analysis results are shown in table 1.

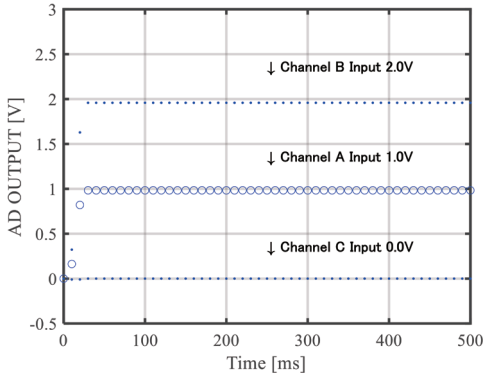

Fig. 14. A/D conversion results of DC voltage inputs

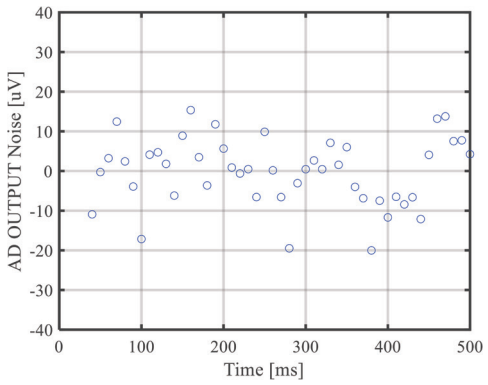

Fig. 15. Deviation of A/D conversion results for channel A

Table 1. Mean and standard deviation of A/D conversion results of DC voltage inputs

Input channel	Input voltage	Averaging length N	Mean of A/D conversion results	Standard deviation of A/D conversion results
Channel A	1.0V	500	0.983V	8.6uVrms
Channel B	2.0V	250	1.958V	14.7uVrms
Channel C	0.0V	250	0.001V	10.0uVrms

The following are the conclusions from figures 14 and 15 and table 1.

A comparison between the input voltages of each channel and the mean of A/D conversion results in table 1 shows that, although there are errors of approximately 1.7%, the results generally exhibit consistency with the input voltages. The multi-channel parallel A/D conversion using an interleaved delta-sigma modulator is considered to be functioning as indented. The errors of 1.7% can be considered to be caused by gain (sensitivity) errors with respect to the input voltages, as the errors are large when the absolute values of the input voltages are large. These errors are considered to be caused by a mismatch between the capacitors for the input signal and the output feedback capacitors in the switched capacitor circuit in figure 11. Parasitic element extraction within the IC circuit revealed that the aforementioned capacitance mismatch was caused by parasitic capacitance. The gain error, which can be corrected through calibration or similar techniques, is not considered a significant issue.

Next, the standard deviation of the A/D conversion results in table 1 is analyzed as noise from A/D conversion. As the standard deviation of the A/D conversion results is approximately 8.67 to 14.7 μV_{rms}, the peak width of noise is approximately 52 to 88 μV, which is six times the standard deviation.

The effective resolution that can be used without noise is derived from the ratio of noise to the full-scale voltage. The prototype circuit is a differential input type with the reference voltage of 3.3 V, meaning that the input voltage range is from -3.3 to +3.3 V and the full-scale voltage is 6.6 V. As the ratio of the peak width of noise to the full-scale voltage is approximately 216 to 217, the effective resolution is estimated to be around 16 to 17 bits.

Furthermore, a noise comparison between channels shows that the value for channel A is smaller than those for channels B and C. As described in Section 3.2, channel A was designed with a higher oversampling ratio compared to other channels, assuming its use with the main sensor. This is considered to have contributed to greater noise reduction.

Finally, we will discuss the reduction of latency between sensors during A/D conversion and power consumption, which were the challenges to be addressed in this prototype.

Regarding latency, the latency that occurs at input channel switching was reduced by achieving multi-channel parallel A/D conversion. The difference in A/D conversion time between multiple channels is approximately 10 to 20 μs, which is almost the same as the sampling period of the delta-sigma modulator and is small enough compared with the data update period of approximately 10 ms. As multiple A/D converters are not used for each channel, the power consumption can also be reduced compared to using commercially available products.

4. Conclusion

In this report, we prototyped and evaluated an interleaved delta-sigma ADC capable of parallel A/D conversion of multiple channels, and confirmed the actual operation of parallel A/D conversion of multiple channels. In terms of accuracy as well, the ability to achieve a 16-bit precision or higher with a data update period of 10 ms suggests that the proposed technique is suitable for a wide range of applications in industrial measuring instruments.

We think this report has demonstrated the effectiveness of custom ICs for design challenges that are difficult to resolve using discrete components. Future work involves focusing on further performance improvements, such as optimizing circuit power consumption and addressing gain errors caused by parasitic capacitance, and we will continue to strengthen and develop IC design techniques to enhance the performance of our products.

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